System and Method for Providing a Redundant Memory Array in a Semiconductor Memory Integrated Circuit

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ABSTRACT OF THE DISCLOSURE

A memory device that has an internal memory array provides timing signals to control the output timing of one or more redundant memory blocks that substitute for defective memory blocks in the internal memory array. In one embodiment, the internal memory array includes a pipelined output stage, and the timing signals ensure that the data is output from the memory devices in the order memory access requests are issued, even when the latency of the redundant memory blocks is less than the latency of the main memory array by up to two clock periods. In one embodiment, a FIFO memory queues the output data of the redundant memory blocks waiting to be output.